**Cell Description:**

This is a standard inverter cell with the following Boolean equation.

**Truth Table:**

|  |  |
| --- | --- |
| A | Y |
| 0 | 1 |
| 1 | 0 |

**Behavioral Verilog:**

The behavioral Verilog for the inverter is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2, 4, and 8).

//Verilog HDL for "Lib6710\_06", "INVXN" "behavioral"

module INVXN ( Y, A );

output Y;

input A;

not \_i0(Y, A);

specify

(A => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| INVX1 | 27.0 | 4.8 |
| INVX2 | 27.0 | 4.8 |
| INVX4 | 27.0 | 4.8 |
| INVX8 | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.261011 | 4.441372 |
| INVX2 | 0.225636 | 4.087162 |
| INVX4 | 0.20974 | 3.927988 |
| INVX8 | 0.19849 | 3.917132 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.208141 | 3.634253 |
| INVX2 | 0.173378 | 3.283945 |
| INVX4 | 0.157781 | 3.127143 |
| INVX8 | 0.14623 | 3.115807 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.353699 | 5.887184 |
| INVX2 | 0.257917 | 4.566921 |
| INVX4 | 0.223438 | 4.095382 |
| INVX8 | 0.210379 | 4.073315 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| INVX1 | 0.267747 | 4.725145 |
| INVX2 | 0.185996 | 3.561277 |
| INVX4 | 0.156828 | 3.151193 |
| INVX8 | 0.145615 | 3.129725 |

**Logic Symbol**

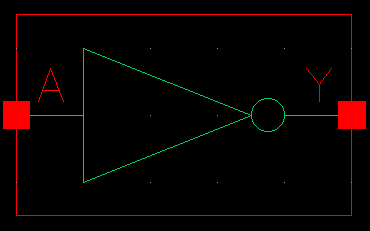
****

Figure 1: Symbol View for the inverter cell.

**CMOS Schematic**The following figure displays the CMOS schematic for the invert cell with a 1 times drive strength (INVX1), all drive strengths have the same schematic with transistor widths that scale by the drive strength factor (i.e. the width of the PMOS in the INVX2 is 6.0μM and the NMOS width is 3.0μM) .

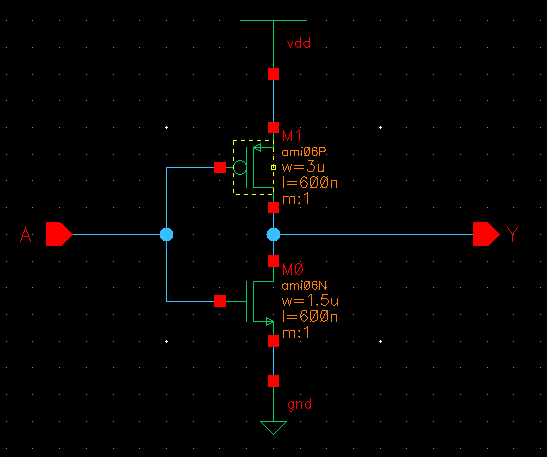
****

Figure 2: CMOS Schematic for the INVX1 cell.

**CMOS Layout:**The following figures display the CMOS layouts for the INV cells.

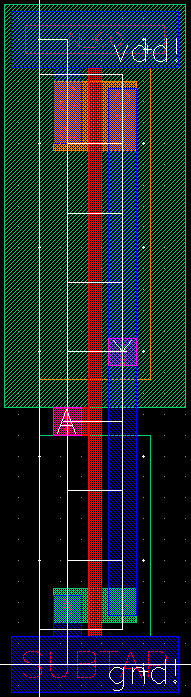
****

Figure 3: CMOS layout for the INVX1 cell.

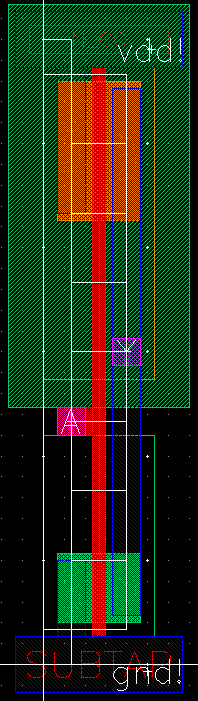
****

Figure 4: CMOS layout for the INVX2 cell.

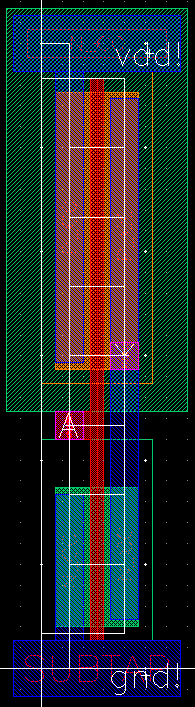
****

Figure 5: CMOS layout for the INVX4 cell.

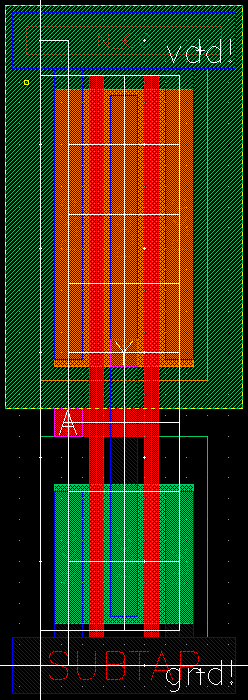
****

Figure 6:CMOS layout for the INVX8 cell.